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Simulation of a ring oscillator with CMOS Inverters

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Contents

Introduction

Electrical oscillators are used within all kinds of electronic systems in the information, communication and sensor technology fields, [5]. For example in radio frequency (RF) communication systems, they are used for frequency translation of information signals and for channel selection, [6]. CMOS inverter ring oscillators offer some valuable advantages like a large tuning range, a large signal swing and a small chip area.

If we consider the unity-gain negative feedback circuit shown in Fig. 1, where

$$\frac{V_{out}}{V_{in}}(s) = \frac{H(s)}{1+H(s)} \quad (1)$$

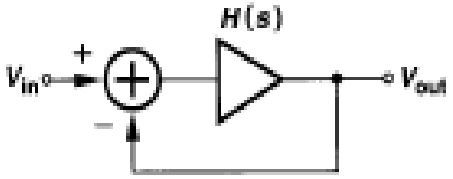


Fig.1. Feedback system

then the circuit may oscillate at ω_0 if the following conditions called the "Barkhausen criteria" are met.

$$|H(j\omega_0)| \geq 1 \quad (2)$$
$$\measuredangle H(j\omega_0) = 180° \quad (3)$$

1. Ring oscillator

A ring oscillator is realized by placing an odd number of open-loop inverting amplifiers in a feedback loop. The simplest type of amplifier that can be used is a simple digital inverter, as shown in Fig. 2. The circuit will oscillate and for each half-period, the signal will propagate around the loop with an inversion. This change will propagate through all three inverters in a time of T/2, at which time the output of the first inverter will change to 0 and after an additional time of T/2 the first inverter's output will change back to 1. Assuming each inverter has a delay of τ_p and that there are N inverters, [1] we then have

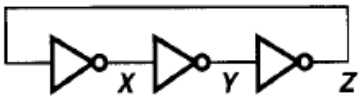


Fig.2. A ring oscillator realized using three digital inverters

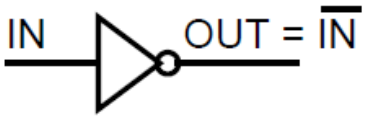
$$\frac{T}{2} = N\tau_p \quad (4)$$

Thus,

$$f_{osc} = \frac{1}{2N\tau_p} \quad (5)$$

2. CMOS Inverter

An inverter is the simplest logic gate which implements the logic operation of negation. A logic symbol and the truth/operation table is shown in Fig.3. Two logic symbols, ‘0’ and ‘1’ are represented by two voltages ‘VL’ and ‘VH’.



IN	OUT	V_{IN}	V_{OUT}
0	1	V_L	V_H
1	0	V_H	V_L

Fig.3. Inverter: symbol and truth table

A CMOS inverter is a circuit which is built from a pair of nMOS and pMOS transistors operating as complementary switches as illustrated in Fig.4. The main advantage of a CMOS inverter over many other solutions is that it is built exclusively out of transistors operating as switches, without any other passive elements like resistors or capacitors, [7]. This inverter will be used in the next chapters as part of a ring oscillator.

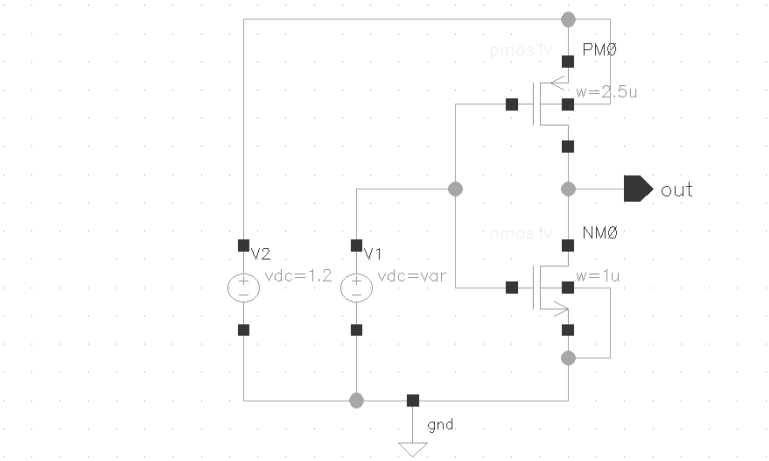


Fig.4. CMOS Inverter circuit in Cadence

The principle of operation is as follows:

1) for small values of the input voltage, VIN, the nMOS transistor is switched off, whereas the pull-up pMOS transistor is switched on and connects the output mode to VDD

2) for large values of the input voltage, VIN, the pMOS transistor is switched off, whereas the pull-down nMOS transistor is switched on and connects the output mode to GND = 0V.

A DC simulation of the CMOS inverter was performed in Cadence Virtuoso ADE L and the transfer and current characteristics were obtained, Fig.5.

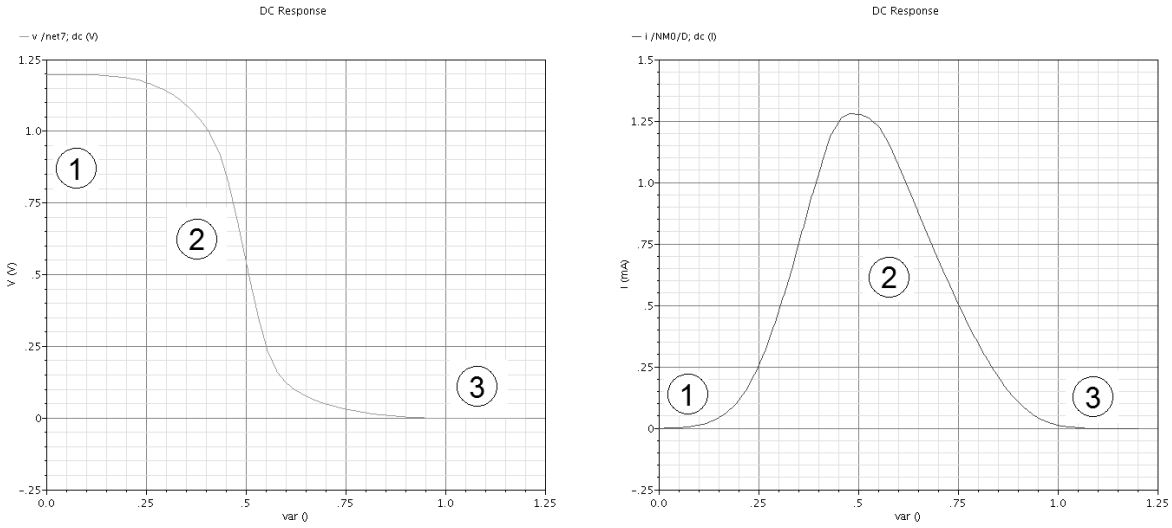


Fig.5. The transfer (left) and current (right) characteristics of a CMOS Inverter

We observe that in regions 1 and 3 no current flows between $V_{DD}$and GND, which means that there is no power dissipation at these stages. This very fact is the reason that all digital circuitry is now build in the CMOS technology. Note that in region 2 there is non-zero current flowing between $V_{DD}$and GND, and some power dissipation, which is converted into heat.

The physical reason for the propagation time delay of a CMOS Inverter is the existence of the parasitic capacitances associated with a MOS transistor. These are parasitic capacitances between the gate and the source or drain of nMOS and pMOS transistors due to overlapping the gate and diffusion regions, the parasitic capacitances between the drains of the transistors and the relevant substrate and the gate capacitance over the gate area. All such capacitances can be combined into an equivalent load capacitance C_L, as illustrated in Fig. 6.

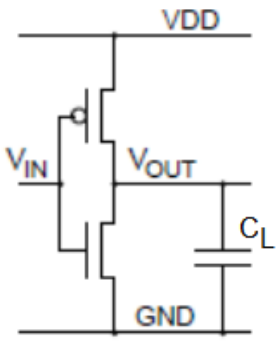


Fig.6. A CMOS inverter with an equivalent load capacitance

3. Design and Layout of a ring oscillator in Cadence

In this section we will present the design, Fig.7, and layout, Fig.8, of a ring oscillator with CMOS Inverters in the gpdk 90nm Version 4.5. technology.

The schematic includes 3 pMOS transistors with the width W=2.5μm and length L=0.1μm and 3 nMOS transistors with W=1μm and L=0.1μm.

For the Layout we chose the transistors with respect to the schematic. We have used for the connections Metal 1, and 3 different VIAs, namely VIA M1-NWELL, VIA M1-PSUB, VIA M1-POv (Metal1-Polysilicon).

The next step is the extraction of the physical parameters of the circuit using Assura RCX.

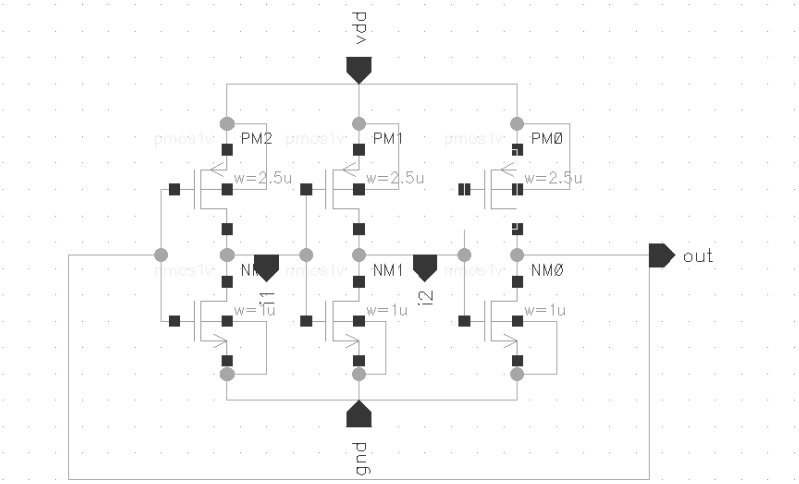


Fig.7. Ring oscillator schematic

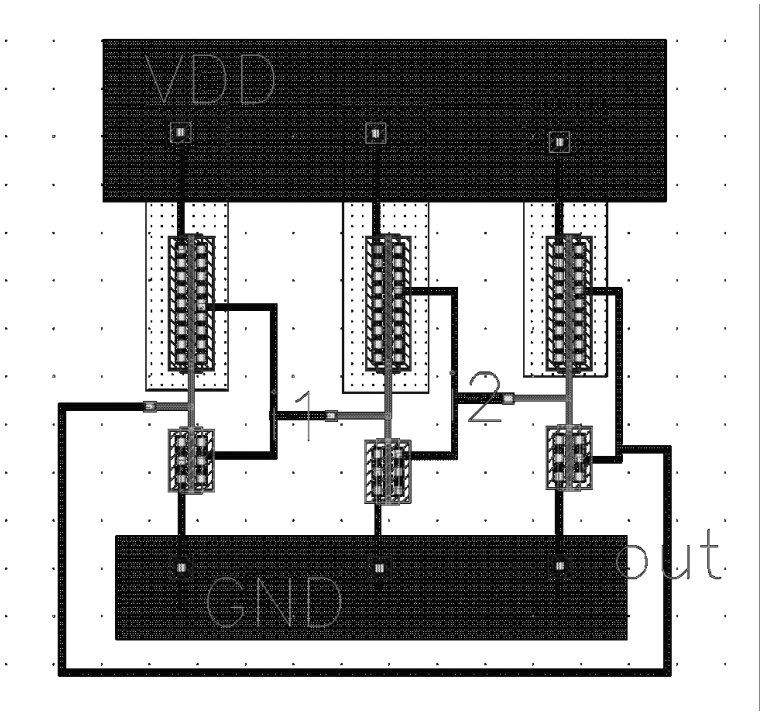


Fig.8. Ring oscillator - layout

4. Estimation of the oscillation frequency and phase noise

Noise is of major concern in oscillators, because introducing even small noise into an oscillator leads to dramatic changes in its frequency spectrum and timing properties. A perfect oscillator would have localized tones at discrete frequencies (i.e.,

harmonics), but any corrupting noise spreads these perfect tones, resulting in high power levels at neighboring frequencies, [6].

In this section, I use the expressions for oscillation frequency and phase noise in single-ended ring oscillators introduced in [4], applying the phase-noise model from [3] in order to estimate the oscillation frequency and phase noise of the designed ring oscillator.

The National Institute of Standards and Technology (www.nist.gov) defines single-side band phase noise as the ratio of power in one phase modulation sideband per Hertz bandwidth, at an offset f Hertz away from the carrier, to the total signal power. Here, f is the offset frequency from the carrier, [8]:

$$L(f_{off}) = \frac{P_s}{P_{ssb}} \quad (6)$$

where P_s is the carrier power and P_{ssb} the sideband power in one Hz bandwidth at an offset frequency f from the center. The SSB phase noise is usually given logarithmically:

$$L(f)\ in\ dBc/Hz = 10\log[L(f)] \quad (7)$$

First we needed to calculate the equivalent load capacitance C_L for the inverter in the 90nm CMOS process. Reference [2] introduces a numerical approach which we will apply to our model.

In Table 1 we've extracted from the spectre model file of the transistors nMOS1v and pMOS1v the necessary parameters needed to estimate the parasitic capacitances. The gate capacitance was computed according to the relation 8, introducing the values of the oxide thickness of the transistors, namely $t_{oxn} = 2.33nm$, $t_{oxp} = 2.48nm$, and the permittivity of SIO_2, $\varepsilon_{ox} = 0.351pF/cm$.

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad (8)$$

Table 1. Transistor parameters

	C_{ox} $(fF/\mu m^2)$	C_O $(fF/\mu m)$	C_j $(fF/\mu m^2)$	m_j	Φ_b (V)	C_{jsw} $(fF/\mu m)$	m_{jsw}	Φ_{bsw} (V)
nMOS1v	15	0.26	0.8	0.222	0.992	0.047	0.01	0.1
pMOS1v	14.1	0.25	0.79	0.331	1.009	0.048	0.01	0.1

Figure 9 shows the schematic of a cascaded inverter pair, which includes all the capacitances influencing the transient response of node V_{OUT}.

The expressions and the values of these capacitances described in Section 2, are presented in Table 2. The wire capacitance was extracted with Assura RCX in the previous section and is approximately C_W=0.05fF.

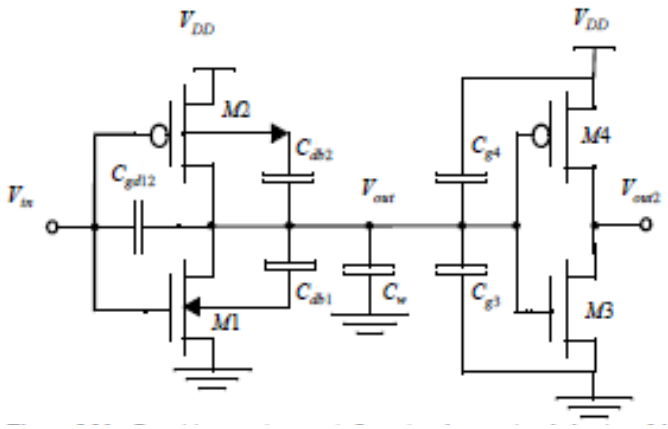


Fig.9. Parasitic Capacitances

Table 2. Calculation of the capacitances

Cap	Relation	Value (fF) (H→L)	Value (fF) (L→H)
C_{gd1}	$2CGD0_n \cdot W_n$	0,52	0,52
C_{gd2}	$2CGD0_p \cdot W_p$	1,25	1,25
C_{db1}	$K_{eqn}AD_nCJ + K_{eqswn}PD_nCJSW$	0,311	0,328
C_{db2}	$K_{eqp}AD_pCJ + K_{eqswp}PD_pCJSW$	0,770	0,707
C_{g3}	$(CGD0_n + CGS0_n)W_n + C_{ox}W_nL_n$	2,02	2,02
C_{g4}	$(CGD0_p + CGS0_p)W_p + C_{ox}W_pL_p$	4,775	4,775
C_W	Aus RCX Extraktion	0.05	0.05
C_L	$\sum$	9.69	9.65

The single-sideband phase-noise due to a white-noise current source is given by [6]

$$L(f_{off}) = \frac{\Gamma_{rms}{}^2}{8\pi^2 f_{off}{}^2} \cdot \frac{\overline{\iota_n{}^2}/\Delta f}{q_{max}{}^2} \quad (9)$$

where $\Gamma_{rms}$is the rms value of the impulse sensitivity function, ISF, $\overline{\iota_n{}^2}/\Delta f$ is the single-sideband power spectral density of the noise current source, f_{off} is the frequency offset from the carrier and q_{max} is given by the relation

$$q_{max} = C_L V_{DD} \quad (10)$$

If the noise sources on different nodes are uncorrelated, the waveform (and hence the ISF) of all the nodes are the same except for a phase shift, assuming identical stages. Therefore, the total phase noise due to all N noise sources is N times the value given by (9).

The relation 13 is used to calculate the rms value of the ISF for the ring oscillator, introducing η=0.75.

$$\Gamma_{rms} = \sqrt{\frac{2\pi^2}{3\eta^3}} \cdot \frac{1}{N^{1.5}} \quad (11)$$

We start with a single-ended CMOS ring oscilltor with equal-length NMOS and PMOS transistors. Assuming that $V_{TN} = |V_{TP}|$, the maximum total channel noise from NMOS and PMOS devices, when both the input and output are at $V_{DD}/2$, is given by

$$\frac{\overline{\iota_n{}^2}}{\Delta f} = 4KT\gamma\mu_{eff}C_{ox}\frac{W_{eff}}{L}\Delta V \quad (12)$$

where

$$W_{eff} = W_n + W_p \quad (13)$$

$$\mu_{eff} = \frac{\mu_n W_n + \mu_p W_p}{W_n + W_p} \quad (14)$$

and ΔV is the gate overdrive in the middle of transition, $\Delta V = (V_{DD}/2) - V_T$.

Assuming $\mu_n W_n + \mu_p W_p$ to make the waveforms symmetric to the first order, the oscillation frequency for a load capacitance $C_L = 9.7fF$ is approximately given by

$$f_0 = \frac{1}{2N\tau_p} = \frac{1}{\eta N(t_r + t_f)} \approx \mu_{eff}C_{ox}\frac{W_{eff}}{8\eta N L q_{max}}\Delta V^2 \quad (15)$$

where t_r and t_f are the rise and fall time, respectively, associated with the maximum slope during a transition.

$$f_0 \approx \frac{(1350\cdot 1 + 480\cdot 2.5)\cdot 10^{-10}\cdot 14.1\cdot 10^{-3}\cdot (0.3)^2}{8\cdot 0.75\cdot 3\cdot 10^{-7}\cdot 9.7\cdot 10^{-15}\cdot 1.2} = 15.44\ GHz \quad (16)$$

Next we calculate the SSB phase noise with an offset frequency f_{off} = 1MHz.

$$L(f_{off}) = 10\log[3 \cdot \frac{16}{9 \cdot \pi^2 \cdot 10^{12}} \cdot \frac{178 \cdot 10^{-24}}{(11.52)^2 \cdot 10^{-30}}] = 10\log\ 0.0302 \cdot 10^{-6} \Longrightarrow$$
$$L(f_{off}) = -75.2dBc/Hz \quad (17)$$

5. Simulation of the ring oscillator

In this chapter we will apply three simulation analyses: a PSS analysis to determine the frequency of oscillation and the influence of parameters such as supply voltage, temperature or load capacitance over the oscillation frequency, a transient analysis for the simulation of the circuit including the parasitic parameters extracted and presented in Section 3 and a PNOISE analysis to determine the phase noise of the designed ring oscillator.

The following schematic has been used for simulations, Fig.10, where the symbol ringosc stands for the ring oscillator designed in section 4.

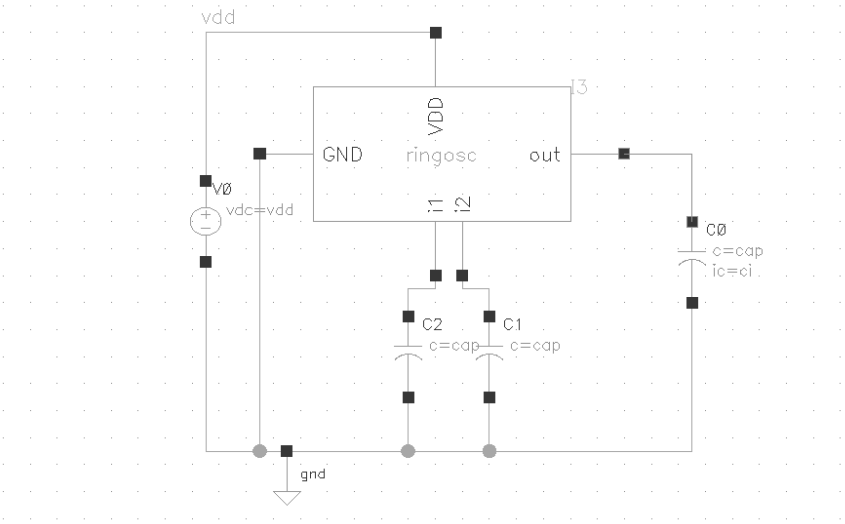


Fig.10. Schematic for simulation

For the PSS analysis I've set as parameters a beat frequency of 4 GHz with respect to the transient analysis, Fig. 11, a conservative accuracy and I've selected the oscillator node and reference. The beat frequency represents the estimate of the oscillation period necessary for the analysis, as described in [9]. The transient analysis had as parameters cap=200 fF and temperature=27°C.

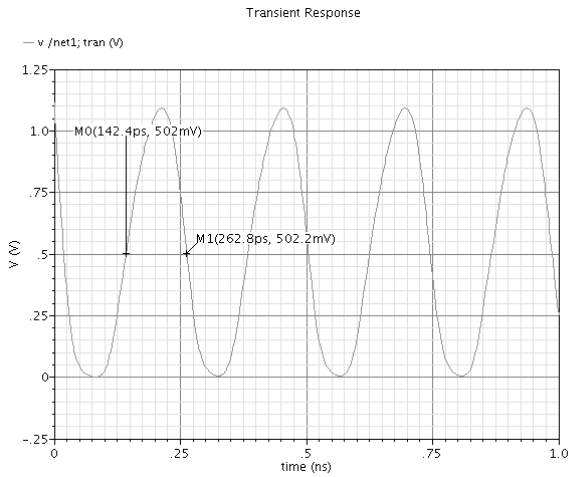


Fig.11. Transient analysis

After performing the first PSS analysis the oscillation frequency resulted to be equal to 4.151 GHz, for a capacitance cap=200f F. In Fig. 12 the output voltage is represented in frequency and time domain.

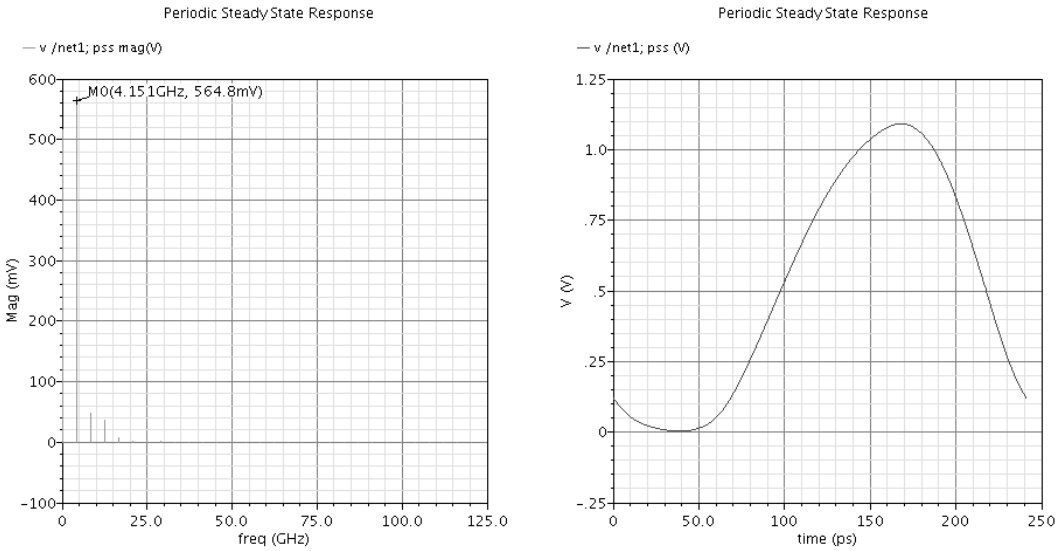


Fig.12. Output voltage in frequency and time domain

In order to determine the influence of the supply voltage over the oscillation frequency, we've simulated the circuit for 2 values of vdd, vdd1=1.2V, vdd2=1V. Figure 13 illustrates that for a smaller value of the supply voltage, the oscillation frequency and voltage magnitude are also smaller, in this case for vdd=1V, f=3.353GHz, V=486.3mV. The reason for the decrease of the oscillation frequency is that the propagation delays of each inverter stages depends proportionally on the supply voltage, as described in [2].

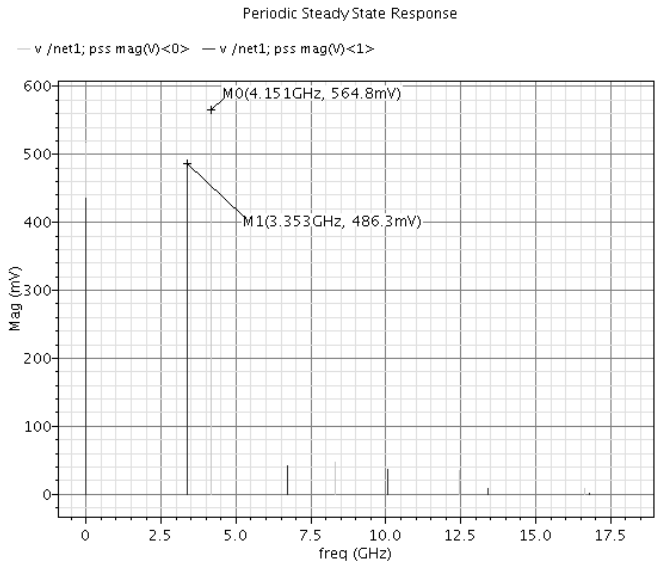


Fig.13. Influence of the supply voltage over the oscillation frequency

For the third PSS analysis, I've used three values for the capacitance, 200 fF, 400 fF, respectively 800 fF. Note that the total output capacitance of a delay element, directly affects the frequency of oscillation with respect to the relation (18), [2].

$$f_{osc} \approx \frac{1}{C_L} \quad (18)$$

This relation is also visible in the simulation in Fig. 14, where the frequency of oscillation decreases 2 times, while the capacitance increases also 2 times. It can also be seen that the output voltage magnitude depends non linearly on the decreasing of the capacitance, for example for cap=800f F V=564.8 mV and for cap=400f F V=563.3 mV.

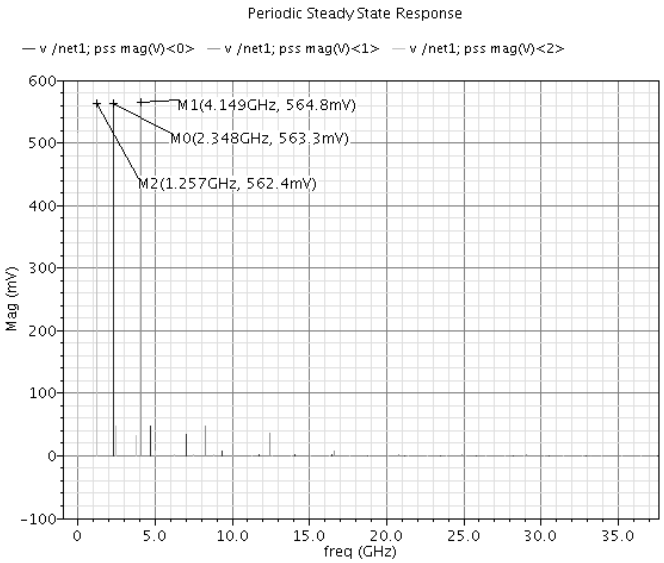


Fig.14. Frequency spectrum for different values of the load capacitance

In Fig. 15 the influence of the temperature over the oscillation frequency of the circuit is illustrated. Two PSS simulations were performed for T1=27˚ C and T2= -27˚C and it resulted that, when the temperature decreases the oscillation frequency increases. In this case for a 54 ˚C temperature decrease, the oscillation frequency has increased with 760MHz.

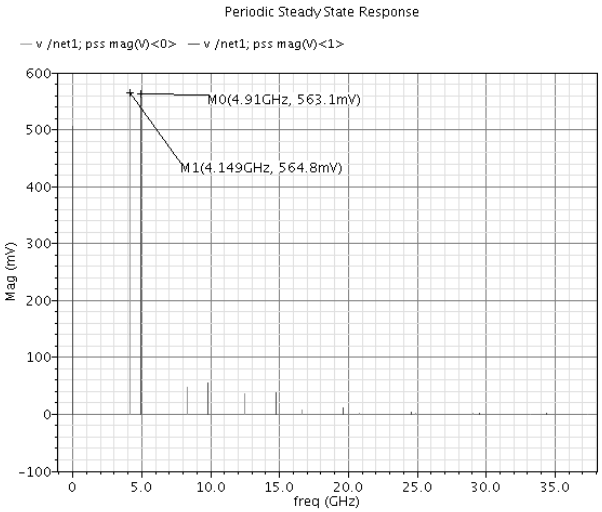


Fig.15. Influence of the temperature over the oscillation frequency

The oscillation frequency is also influenced by the physical parameters of the circuit, in this case a ring oscillator built with 3 inverter stage. In section 3, the physical parameters were extracted for the designed oscillator using Assura RCX Extractor in Cadence. The extraction is in the form of a new netlist of the circuit

which includes the transistor parameters and also the parasitic parameters, namely parasitic resistors and capacitors, of the designed layout. A transient analysis was performed to illustrate the effect of these parameters on the oscillation frequency of the circuit, Fig. 16.

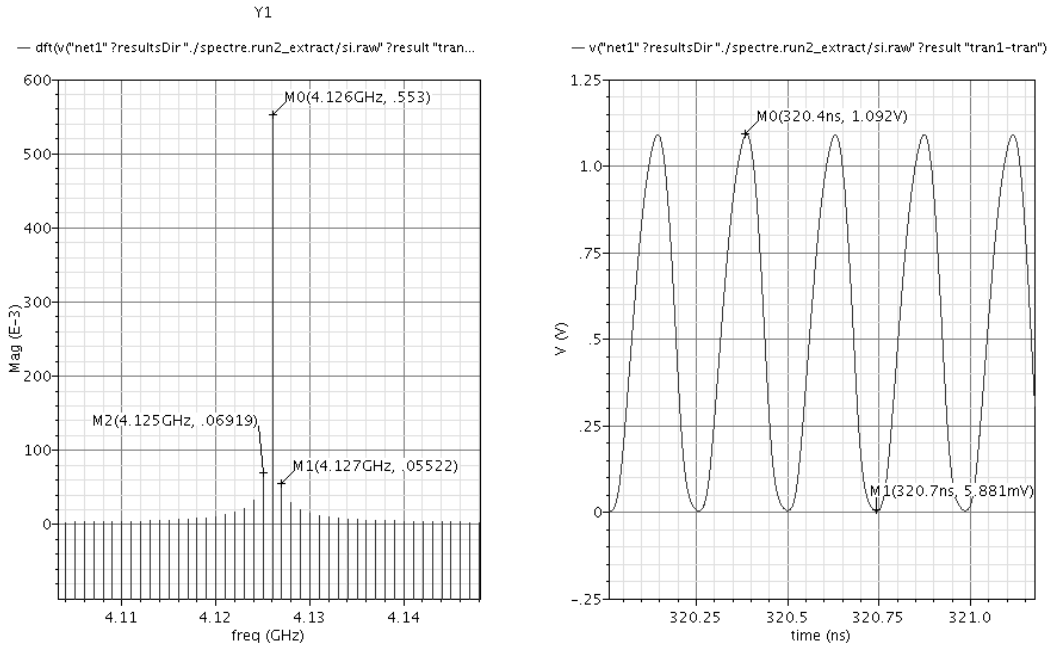


Fig.16. Output voltage in frequency and time domain including parasitic parameters

Figure 17 shows the differences between the simulation of the circuit without (left) and with (right) parasitic parameters. Note that the oscillation frequency decreases when the parasitic resistors and capacitors are taken into account.

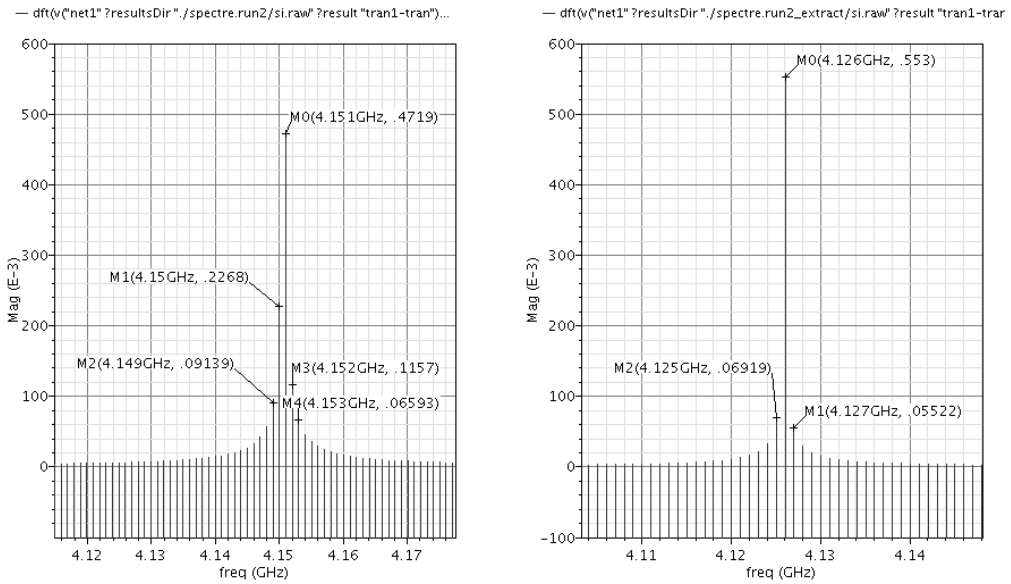


Fig.17. Oscillation frequency without (left) with parasitic parameters (right)

The next simulation intends to verify the result we've obtained by the estimation of the oscillation frequency, Fig.18. It may be observed, that simulating the circuit with a load capacitance of 10fF, we obtain a frequency f=15.36 GHz, while from the manual calculations we've obtained a frequency f=15.44 GHz.

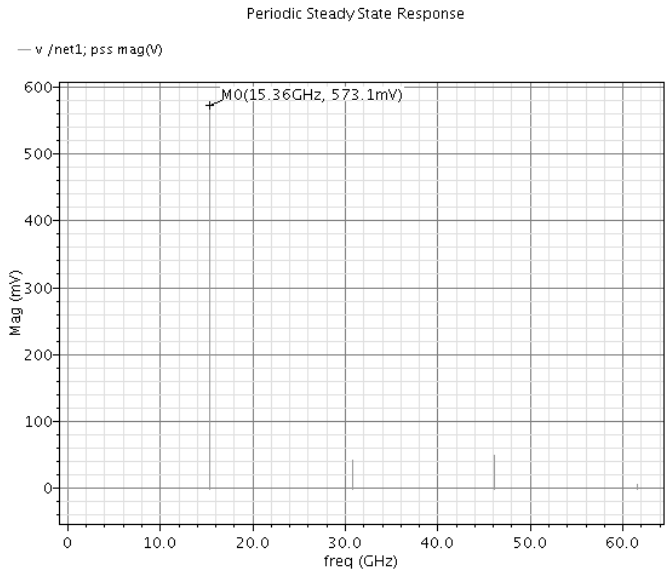


Fig.18. Oscillation frequency for a load capacitance of 10fF

The estimation of the phase noise -75.2 dBc/Hz is also close to the result we've obtained by performing a phase noise simulation, Fig.19. In the case of the simulation, we've obtained a phase noise of $L = -76.52\ dBc/Hz$ by an offset of approximately 1MHz.

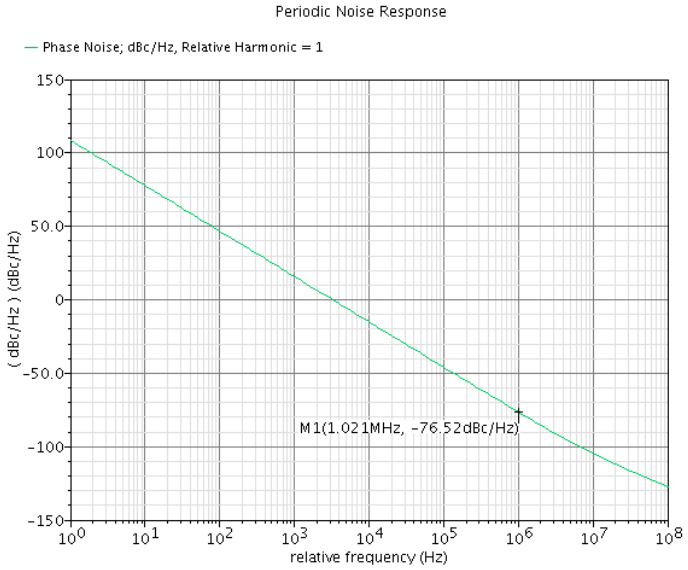


Fig.19. Phase noise by a frequency offset f=1MHz

Conclusions

1. This paper presents theoretical aspects for the design and simulation of a ring oscillator with CMOS inverters.

2. We've designed the schematic and layout for a ring oscillator with 3 inverter stages in the gpdk90nm technology, and we've extracted the parasitic parameters with Assura RCX.

3. We've estimated the frequency of oscillation and the phase noise for the designed oscillator and we've compared these results with those obtained from simulations.

4. PSS analyses were performed in order to determine the frequency of oscillation and the influence of parameters such as supply voltage, temperature or load capacitance over the oscillation frequency. A transient analysis was performed to illustrate the effects of the parasitic parameters over the oscillation frequency.

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